

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael Goessel et al.	Examiner:	Daniel F. McMahon
Serial No.:	10/577,288	Group Art Unit:	2117
Filed:	April 24, 2006	Docket No.:	I431.135.101/FIN516PCT/US
Title:	EVALUATION CIRCUIT AND METHOD FOR DETECTING AND/OR LOCATING FAULTY DATA WORDS IN A DATA STREAM T _N		

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Please consider the following remarks during the Pre-Appeal Brief Conference. As these remarks outline a clear legal or factual deficiency in the rejections, Applicant submits that the Pre-Appeal Brief Request for Review is appropriate.

Claim Rejections under 35 U.S.C. § 103

The Office Action rejected claims 35, 51, and 55 under 35 U.S.C. 103(a) as allegedly being unpatentable over Hasegawa et al. U.S. Publication 2004/0246337 (“Hasegawa”), in view of Wu, U.S. Patent 5,831,992 (“Wu”) and Borden et al. U.S. Patent 5,790,561 (“Borden”). Applicants respectfully contend these rejections are improper and thus should be withdrawn..

One criterion that must be satisfied to establish a *prima facie* case of obviousness is the reference or combined references must teach or suggest all of the claim limitations. *In re Royka*, 490 F.2d 981 [180 USPQ 580] (C.C.P.A. 1974). Claim 35 includes,

the first linear automaton circuit and the second linear automaton circuit are designed such that a first signature and a second signature, respectively, is calculated of each data word of the n successive data words y(1), ..., y(n)

The Office Action admits that neither Hasegawa nor Wu disclose at least this claim element, but relies on an alleged disclosure in Borden.

Borden discloses a fault isolation system for use in an integrated circuit that includes a special “user register” that is formed from a series connected chain of multiple input shift registers (MISR). Figure 5 of Borden is reproduced below.

Pre-Appeal Brief Request for Review

Applicant: Michael Goessel et al.

Serial No.: 10/577,288

Filed: April 24, 2006

Docket No.: I431.135.101/FIN516PCT/US

Title: EVALUATION CIRCUIT AND METHOD FOR DETECTING AND/OR LOCATING FAULTY DATA WORDS IN A DATA STREAM T_N

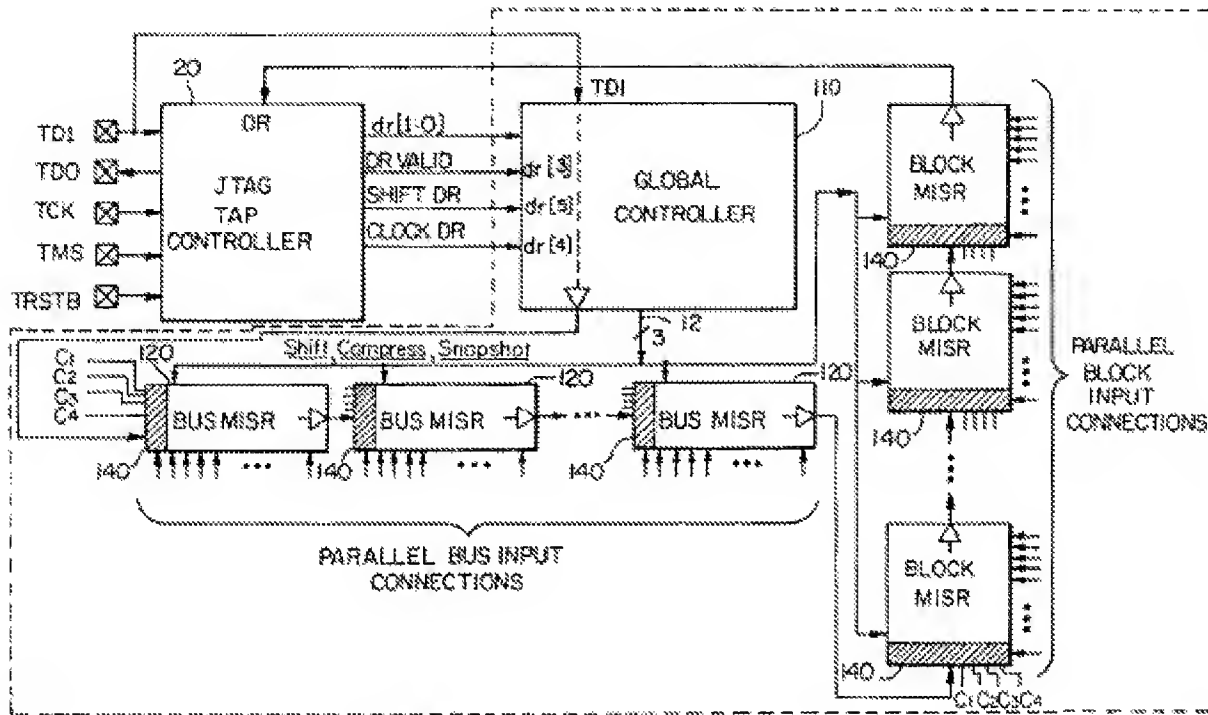


FIG. 5

A tap controller 20 operates a plurality of MISRs 120, 130 via a unique global controller 110 and a corresponding plurality of local controllers 140. (Reference number 130 does not appear to be included in Figure 5, but Borden notes that there are Bus MISRs 120 and Block MISRs 130 at col. 4, ll. 5-6).

In response to Applicants' remarks filed January 31, 2011, the Advisory Action states on the continuation sheet, "Borden discloses: in a compress mode, generating a first and second signature (column 6, lines 8-10), which is calculated for each successive data word (column 6, lines 11-13."

The first cited portion, column 6, lines 8-12, reads as follows, "... of the next stage. Subsequently, the result is passed to the slave latch 220 and made available to the XOR gate 240 of the next stage. This process is accomplished with the global..." This passage of Borden refers to Figure 8 thereof, which illustrates "a circuit schematic illustrating 3 of the 33 stages in a

Pre-Appeal Brief Request for Review

Applicant: Michael Goessel et al.

Serial No.: 10/577,288

Filed: April 24, 2006

Docket No.: I431.135.101/FIN516PCT/US

Title: EVALUATION CIRCUIT AND METHOD FOR DETECTING AND/OR LOCATING FAULTY DATA WORDS IN A DATA STREAM T_N

preferred bus MISR 120 or a block MISR 130.” Col. 3, ll. 4-5. Figure 8 of Borden is reproduced below.

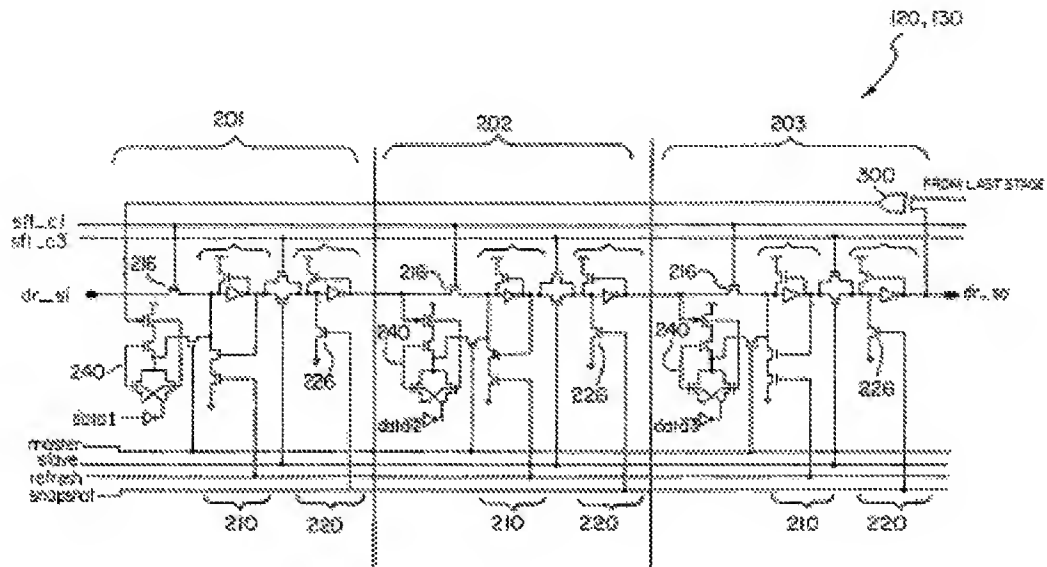


FIG. 8

Lines 11-13 of column 6, together with Figure 8 of Borden merely appear to discuss successively passing data from one stage to another – from an XOR gate 210 to a slave latch 220 then to the next XOR gate. There is no explicit mention of calculating a first signature and a second signature by respective different stages of the MISR, of each data word of the *n* successive data words. Rather than calculating two separate signatures for each data word, as recited in claim 35, the cited portions of Borden appear to teach successively altering data as it passes from one stage to the next.

Moreover, claim 35 states that the first and second linear automation circuits are defined by respective equations. In contrast, the structure of the MISR stages 201, 202, 203 shown in Figure 8 of Borden appear to be identical. Since claim 35 recites the first and second (different) linear automation circuits calculating respective first and second signatures for each data word, there would be no reason for one skilled in the art to even consider the teachings of Borden, where *identical* MISR stages successively receive and alter data.

Pre-Appeal Brief Request for Review

Applicant: Michael Goessel et al.

Serial No.: 10/577,288

Filed: April 24, 2006

Docket No.: I431.135.101/FIN516PCT/US

Title: EVALUATION CIRCUIT AND METHOD FOR DETECTING AND/OR LOCATING FAULTY DATA WORDS IN A DATA STREAM T_N

Further, the Office Action states that Hasegawa discloses a first linear automaton circuit and a second linear automaton circuit connected in parallel as recited in claim 35, citing Figure 4 of Hasegawa. In the continuation page of the Advisory Action, the Examiner explains,

Element 16 and 2 are clearly connected in parallel, the output of elements 17a-n are connected to element 16 Dpa-n (figure 4) and element 2 Dpa-n (figure 5). One of ordinary skill in the art would recognize that in an evaluation circuit, two elements which share a common input connection are connected in parallel.

However, it appears that elements 16 and 2 of Hasegawa do not receive data in parallel. Instead, *either* block 16 or block 2 receives data 17, depending on the mode. Hasegawa teaches in the Brief Description of Drawings section that Figure 4 shows a configuration “in failure determination mode” [0012] and Figure 4 shows a configuration “in failure scan determination mode.” [0013]. Thus, blocks 16 and 2 appear to receive data individually depending on the configuration mode. See, Hasegawa at para. [0064]. There is no disclosure or illustration identified in the Office Action where Hasegawa teaches “a common input connection” as alleged in the Advisory Action.

Since the cited references alone or in combination fail to disclose each claim element, the Office Action fails to establish *prima facie* obviousness of claim 35. As such, claim 35, and claims 51, 52 and 55 dependent thereon, are in condition for allowance.

The Office Action rejected claims 36, 37, 39, 41-45, and 48-50 and 56-58 under 35 U.S.C. 103(a) as allegedly being unpatentable over Hasegawa, Wu, and Borden, in view of additional references. These claims all depend on claim 35 and are therefore allowable for at least the same reasons.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103 rejection to the claims, and request allowance of these claims.

Pre-Appeal Brief Request for Review

Applicant: Michael Goessel et al.

Serial No.: 10/577,288

Filed: April 24, 2006

Docket No.: I431.135.101/FIN516PCT/US

Title: EVALUATION CIRCUIT AND METHOD FOR DETECTING AND/OR LOCATING FAULTY DATA WORDS IN A DATA STREAM T_N

CONCLUSION

In view of the above, Applicant respectfully submits that all of the pending claims are in form for allowance. Therefore, reconsideration and withdrawal of the rejections and allowance of the claims are respectfully requested.

Any inquiry regarding this Pre-Appeal Brief Request for Review should be directed to Mark L. Gleason at Telephone No. (612) 767-2503, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Dicke, Billig & Czaja
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402

Respectfully submitted,

Michael Goessel et al.,

By their attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-2000
Facsimile: (612) 573-2005

Date: 02/28/2011

MLG:cms

/Mark L. Gleason/

Mark L. Gleason

Reg. No. 39,998